

9.2.2 T-Bird Tail Lights

We described and designed a “T-bird tail-lights” state machine in Section 7.5. Table 9-20 is an equivalent VHDL program for the T-bird tail-lights machine. The state transitions in this machine are defined exactly the same as in the state diagram of Figure 7-64 on page 589. The machine uses an output-coded state assignment, taking advantage of the fact that the tail-light output values are different in each state.

Table 9-20 VHDL program for the T-bird tail-lights machine.

```
entity Vtbird is
  port ( CLOCK, RESET, LEFT, RIGHT, HAZ: in STD_LOGIC;
        LIGHTS: buffer STD_LOGIC_VECTOR (1 to 6) );
end;

architecture Vtbird_arch of Vtbird is
  constant IDLE: STD_LOGIC_VECTOR (1 to 6) := "000000";
  constant L3  : STD_LOGIC_VECTOR (1 to 6) := "111000";
  constant L2  : STD_LOGIC_VECTOR (1 to 6) := "110000";
  constant L1  : STD_LOGIC_VECTOR (1 to 6) := "100000";
  constant R1  : STD_LOGIC_VECTOR (1 to 6) := "000001";
  constant R2  : STD_LOGIC_VECTOR (1 to 6) := "000011";
  constant R3  : STD_LOGIC_VECTOR (1 to 6) := "000111";
  constant LR3 : STD_LOGIC_VECTOR (1 to 6) := "111111";
begin
  process (CLOCK)
  begin
    if CLOCK'event and CLOCK = '1' then
      if RESET = '1' then LIGHTS <= IDLE; else
        case LIGHTS is
          when IDLE => if HAZ='1' or (LEFT='1' and RIGHT='1') then LIGHTS <= LR3;
                       elsif LEFT='1'                               then LIGHTS <= L1;
                       elsif RIGHT='1'                             then LIGHTS <= R1;
                       else                                         LIGHTS <= IDLE;
          end if;
          when L1  => if HAZ='1' then LIGHTS <= LR3; else LIGHTS <= L2; end if;
          when L2  => if HAZ='1' then LIGHTS <= LR3; else LIGHTS <= L3; end if;
          when L3  => LIGHTS <= IDLE;
          when R1  => if HAZ='1' then LIGHTS <= LR3; else LIGHTS <= R2; end if;
          when R2  => if HAZ='1' then LIGHTS <= LR3; else LIGHTS <= R3; end if;
          when R3  => LIGHTS <= IDLE;
          when LR3 => LIGHTS <= IDLE;
          when others => null;
        end case;
      end if;
    end if;
  end process;
end Vtbird_arch;
```