

Cntr: Fun with the 74x163 Binary Counter

Although the '163 is a modulo-16 counter, it can be made to count in a modulus less than 16 by using the CLR_L or LD_L input to shorten the normal counting sequence. For example, Figure Cntr-1 shows one way of using the '163 as a modulo-11 counter. The RCO output, which detects state 15, is used to force the next state to 5, so that the circuit will count from 5 to 15 and then start at 5 again, for a total of 11 states per counting cycle.

A different approach for modulo-11 counting with the '163 is shown in Figure Cntr-2. This circuit uses a NAND gate to detect state 10 and force the next state to 0. Notice that only a 2-input gate is used to detect state 10 (binary 1010). Although a 4-input gate would normally be used to detect the condition $CNT10 = Q3 \cdot Q2' \cdot Q1 \cdot Q0'$, the 2-input gate takes advantage of the fact that no other state in the normal counting sequence of 0–10 has $Q3 = 1$ and $Q1 = 1$. In general, to detect state N in a binary counter that counts from 0 to N , we need to AND only the state bits that are 1 in the binary encoding of N .

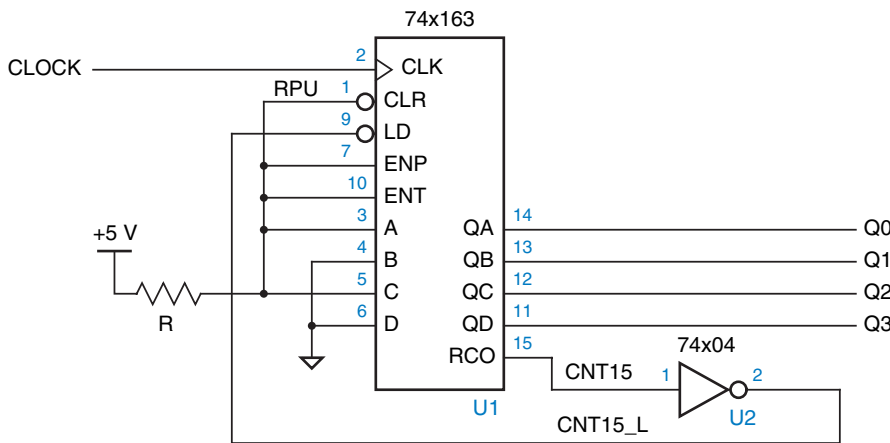


Figure Cntr-1
Using the 74x163 as a modulo-11 counter with the counting sequence 5, 6, ..., 15, 5, 6,

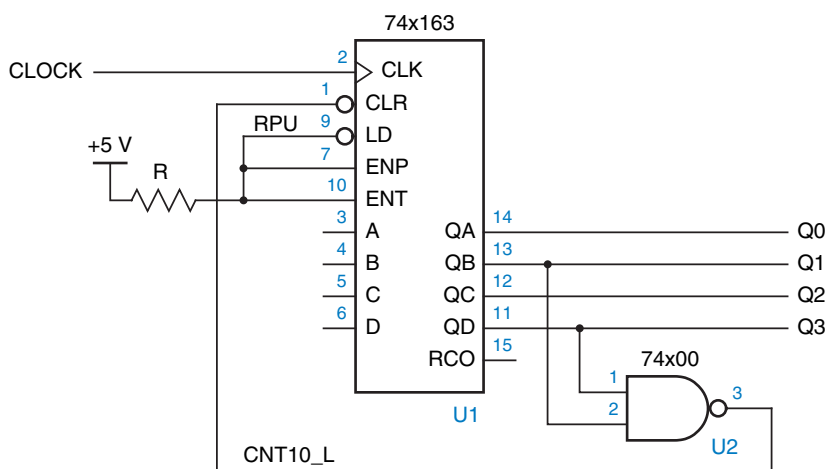


Figure Cntr-2
Using the 74x163 as a modulo-11 counter with the counting sequence 0, 1, 2, ..., 10, 0, 1,

Supplementary material to accompany *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly. ISBN 0-13-186389-4. © 2006 Pearson Education, Inc., Upper Saddle River, NJ. All rights reserved.

This material is protected under all copyright laws as they currently exist. No portion of this material may be reproduced, in any form or by any means, without permission in writing by the publisher.

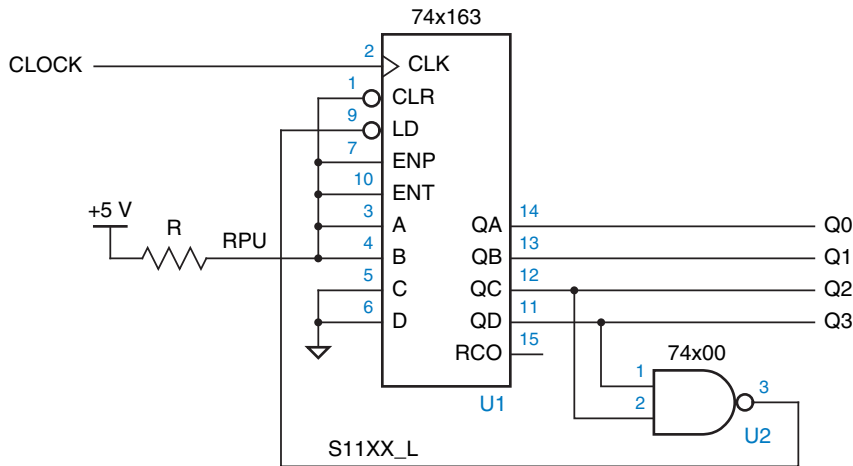
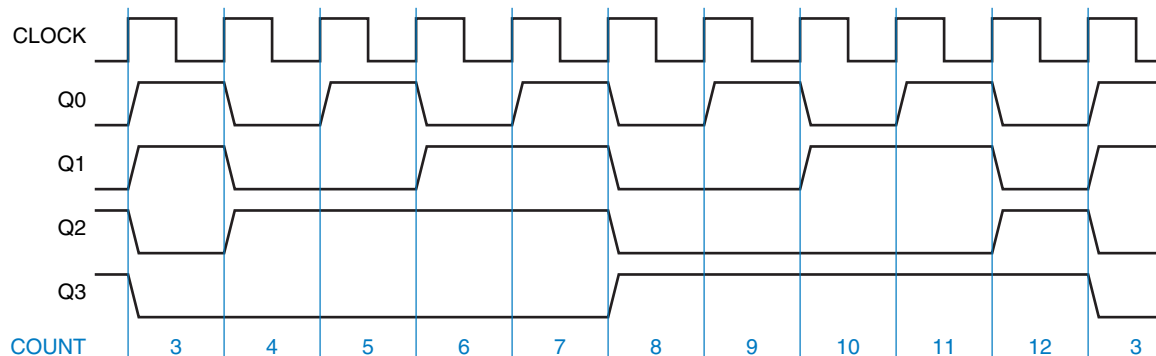


Figure Cntr-3
A 74x163 used as an excess-3 decimal counter.

There are many other ways to make a modulo-11 counter using a '163. The choice of approach—one of the preceding or a combination of them (as in Exercise 8.35)—depends on the application. As another example, in Section 2.10 we promised to show you how to build a circuit that counts in the excess-3 decimal code, shown in Table 2-9 on page 49. Figure Cntr-3 shows the connections for a '163 to count in the excess-3 sequence. A NAND gate detects state 1100 and forces 0011 to be loaded as the next state. Figure Cntr-4 shows the resulting timing waveforms. Notice that the Q3 output has a 50% duty cycle, which may be desirable for some applications.

A binary counter with a modulus greater than 16 can be built by cascading 74x163s. Figure Cntr-5 shows the general connections for such a counter. The CLK, CLR_L, and LD_L inputs of all the '163s are connected in parallel, so that all of them count or are cleared or loaded at the same time. A master count-enable (CNTEN) signal is connected to the low-order '163. The RCO4 output is asserted if and only if the low-order '163 is in state 15 *and* CNTEN is asserted; RCO4 is connected to the enable inputs of the high-order '163. Thus, both the

Figure Cntr-4 Timing waveforms for the '163 used as an excess-3 decimal counter.



Supplementary material to accompany *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly. ISBN 0-13-186389-4. © 2006 Pearson Education, Inc., Upper Saddle River, NJ. All rights reserved. This material is protected under all copyright laws as they currently exist. No portion of this material may be reproduced, in any form or by any means, without permission in writing by the publisher.

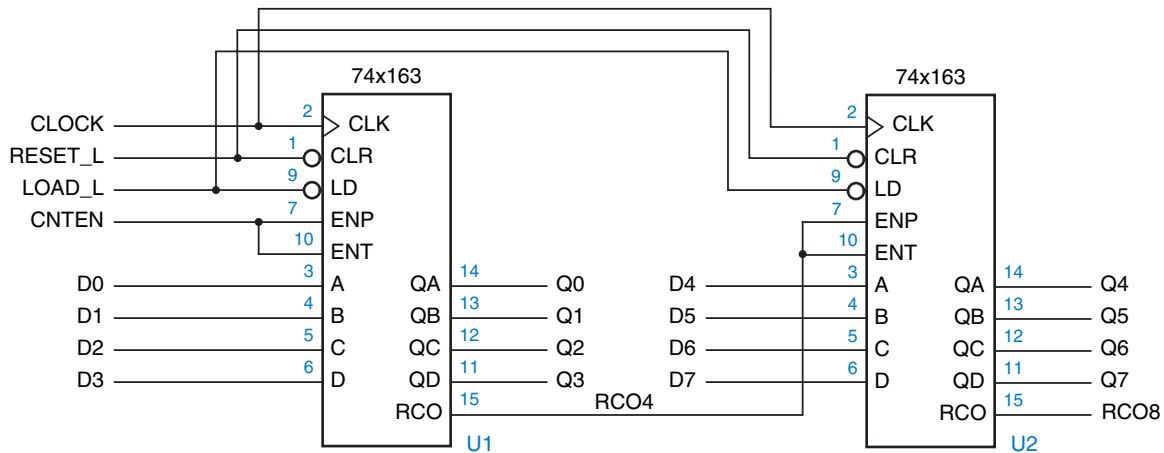


Figure Cntr-5 General cascading connections for 74x163-based counters.

carry information and the master count-enable ripple from the output of one 4-bit counter stage to the next. Like the synchronous serial counter of Figure 8-25, this scheme can be extended to build a counter with any desired number of bits; the maximum counting speed is limited by the propagation delay of the ripple carry signal through all of the stages (but see Exercise 8.37).

Even experienced digital designers are sometimes confused about the difference between the ENP and ENT enable inputs of the '163 and similar counters, since both must be asserted for the counter to count. However, a glance at the '163's internal logic diagram, Figure 8-28 on page 714, shows the difference quite clearly—ENT goes to the ripple carry output as well. In many applications this distinction is important.

For example, Figure Cntr-6 uses two '163s as a modulo-193 counter that counts from 63 to 255. The MAXCNT output detects state 255 and stops the counter until GO_L is asserted. When GO_L is asserted, the counter is reloaded with 63 and counts up to 255 again. (Note that the value of GO_L is relevant only when the counter is in state 255.) To keep the counter stopped, MAXCNT must be asserted in state 255 even while the counter is stopped. Therefore, the low-order counter's ENT input is always asserted, its RCO output is connected to the high-order ENT input, and MAXCNT detects state 255 even if CNTEN is not asserted (compare with the behavior of RCO8 in Figure Cntr-5). To enable counting, CNTEN is connected to the ENP inputs in parallel. A NAND gate asserts RELOAD_L to go back to state 63 only if GO_L is asserted and the counter is in state 255. The counter also goes to state 63 when RESET_L is asserted.

Supplementary material to accompany *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly.
ISBN 0-13-186389-4. © 2006 Pearson Education, Inc., Upper Saddle River, NJ. All rights reserved.

This material is protected under all copyright laws as they currently exist. No portion of this material may be reproduced, in any form or by any means, without permission in writing by the publisher.

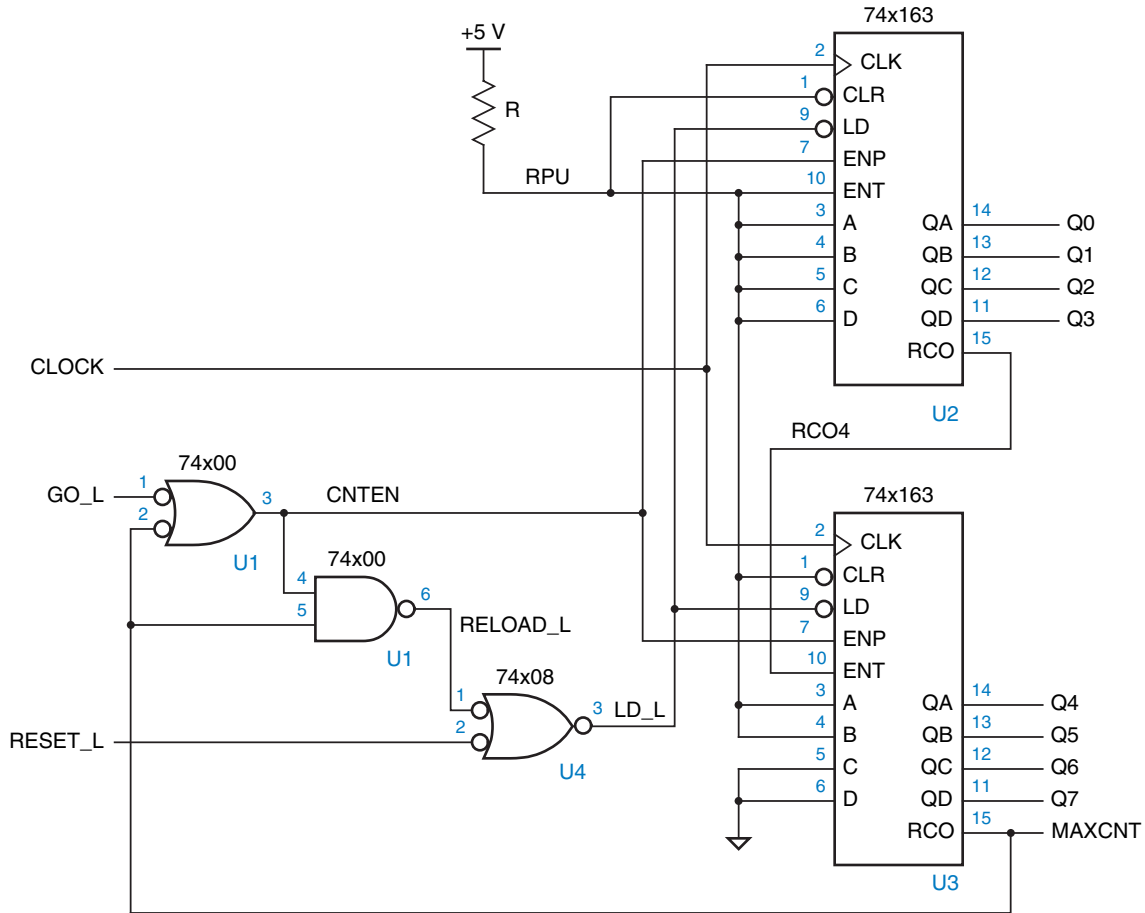


Figure Cntr-6 Using 74x163s as a modulo-193 counter with the counting sequence 63, 64, ..., 255, 63, 64,

Exercises

- Cntr.1** What is the behavior of the counter circuit of Figure Cntr-2 if it is built using a 74x161 instead of a 74x163?
- Cntr.2** What is the behavior of the counter circuit of Figure Cntr-2 if the bottom input of U2 is connected to Q2 instead of Q1?
- Cntr.3** Design a combination-lock machine according to the state table of Table 7-11 on page 568 using a single 74x163 counter and combinational logic for the LD_L, CLR_L, and A–D inputs of the '163. Use counter values 0–7 for states A–H.

Supplementary material to accompany *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly. ISBN 0-13-186389-4. © 2006 Pearson Education, Inc., Upper Saddle River, NJ. All rights reserved.

This material is protected under all copyright laws as they currently exist. No portion of this material may be reproduced, in any form or by any means, without permission in writing by the publisher.

Cntr.4 A digital designer (the author!) was asked at the last minute to add new functionality to a PCB that had room for just one more 16-pin MSI IC. The PCB already had a 16-MHz clock signal, MCLK, and a spare microprocessor-controlled select signal, SEL. The designer was asked to provide a new clock signal, UCLK, whose frequency would be 8 MHz or 4 MHz depending on the value of SEL. To make things worse, the PCB had no spare SSI gates, and UCLK was required to have a 50% duty cycle at both frequencies. It took the designer about five minutes to come up with a circuit. Now it's your turn to do the same. (*Hint*: The designer had long considered the 74x163 to be the fundamental building block of tricky sequential-circuit design.) What if the output needed to be capable of generating 8, 4, or 2 MHz, based on two SEL lines, but the 50% duty cycle was not required?

Supplementary material to accompany *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly.
ISBN 0-13-186389-4. © 2006 Pearson Education, Inc., Upper Saddle River, NJ. All rights reserved.

This material is protected under all copyright laws as they currently exist. No portion of this material may be reproduced, in any form or by any means, without permission in writing by the publisher.