

## TTL: Transistor-Transistor-Logic Topics

The most commonly used bipolar logic family is transistor-transistor logic. Actually, there are many different TTL families, with a range of speed, power consumption, and other characteristics. The circuit examples in this section are based on a representative TTL family, Low-power Schottky (LS or LS-TTL).

TTL families use basically the same logic levels as the TTL-compatible CMOS families in Section 3.8. We'll use the following definitions of LOW and HIGH in our discussions of TTL circuit behavior:

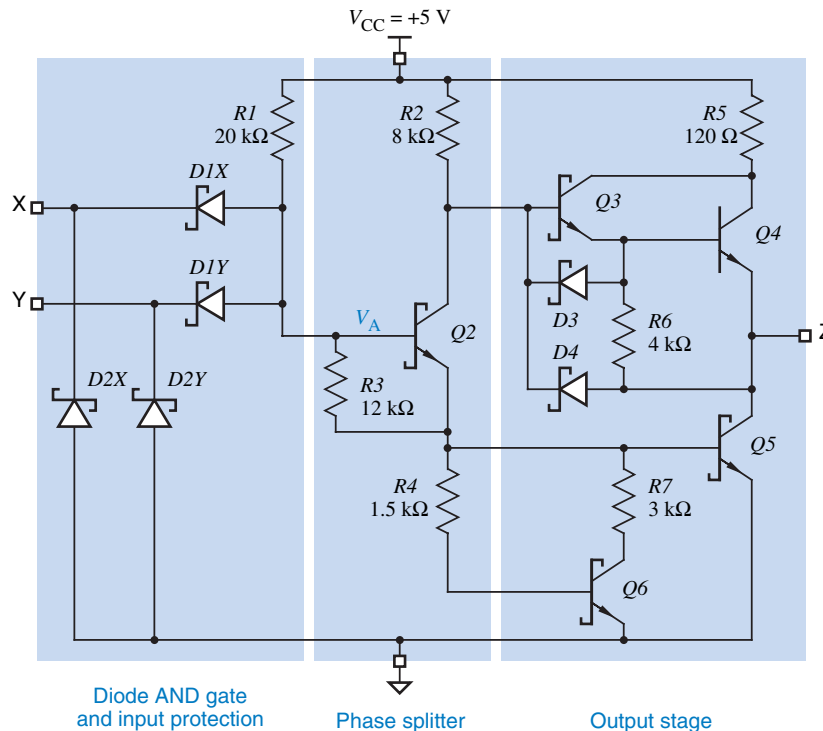
**LOW** 0–0.8 volts.

**HIGH** 2.0–5.0 volts.

### TTL.1 Basic TTL NAND Gate

The circuit diagram for a 2-input LS-TTL NAND gate, part number 74LS00, is shown in Figure TTL-1. The NAND function is obtained by combining a diode AND gate with an inverting buffer amplifier. The circuit's operation is best understood by dividing it into the three parts that are shown in the figure and discussed in the next three paragraphs:

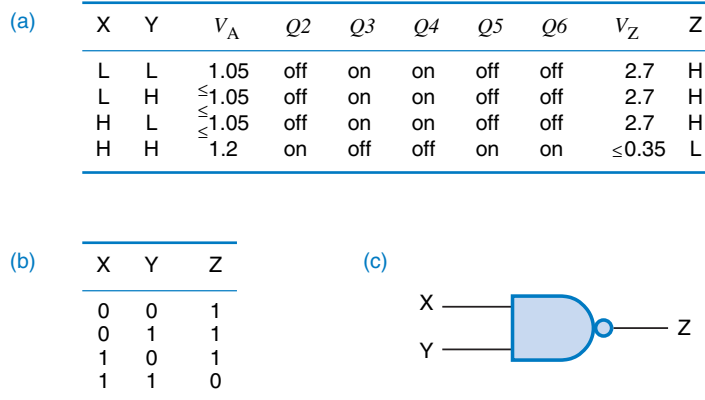
- Diode AND gate and input protection.
- Phase splitter.
- Output stage.



**Figure TTL-1**  
Circuit diagram of  
2-input LS-TTL  
NAND gate.

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**Figure TTL-2**  
Functional operation of a TTL two-input NAND gate:  
(a) function table;  
(b) truth table;  
(c) logic symbol.

Diodes  $D1X$  and  $D1Y$  and resistor  $R1$  in Figure TTL-1 form a *diode AND gate*, as in Section Diode.2. *Clamp diodes*  $D2X$  and  $D2Y$  do nothing in normal operation, but limit undesirable negative excursions on the inputs to a single diode-drop. Such negative excursions may occur on HIGH-to-LOW input transitions as a result of transmission-line effects, discussed in Section Zo.

*diode AND gate*  
*clamp diode*

Transistor  $Q2$  and the surrounding resistors form a *phase splitter* that controls the output stage. Depending on whether the diode AND gate produces a “low” or a “high” voltage at  $V_A$ ,  $Q2$  is either cut off or turned on.

*phase splitter*

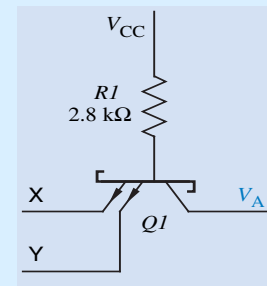
The *output stage* has two transistors,  $Q4$  and  $Q5$ , only one of which is on at any time. The TTL output stage is sometimes called a *totem-pole* or *push-pull output*. Similar to the  $p$ -channel and  $n$ -channel transistors in CMOS,  $Q4$  and  $Q5$  provide active pull-up and pull-down to the HIGH and LOW states, respectively.

*output stage*  
*totem-pole output*  
*push-pull output*

The functional operation of the TTL NAND gate is summarized in Figure TTL-2(a). The gate does indeed perform the NAND function, with the truth table and logic symbol shown in (b) and (c). TTL NAND gates can be designed with any desired number of inputs simply by changing the number of diodes in the diode AND gate in the figure. Commercially available TTL NAND gates have as many as 13 inputs. A TTL inverter is designed as a 1-input NAND gate, omitting diodes  $D1Y$  and  $D2Y$  in Figure TTL-1.

**WHERE IN THE WORLD IS Q1?**

Notice that there is no transistor  $Q1$  in Figure TTL-1, but the other transistors are named in a way that’s traditional; some TTL devices do in fact have a transistor named  $Q1$ . Instead of diodes like  $D1X$  and  $D1Y$ , these devices use a multiple-emitter transistor  $Q1$  to perform logic. This transistor has one emitter per logic input, as shown in the figure to the right. Pulling any one of the emitters LOW is sufficient to turn the transistor ON and thus pull  $V_A$  LOW.



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**CURRENT SPIKES AGAIN**

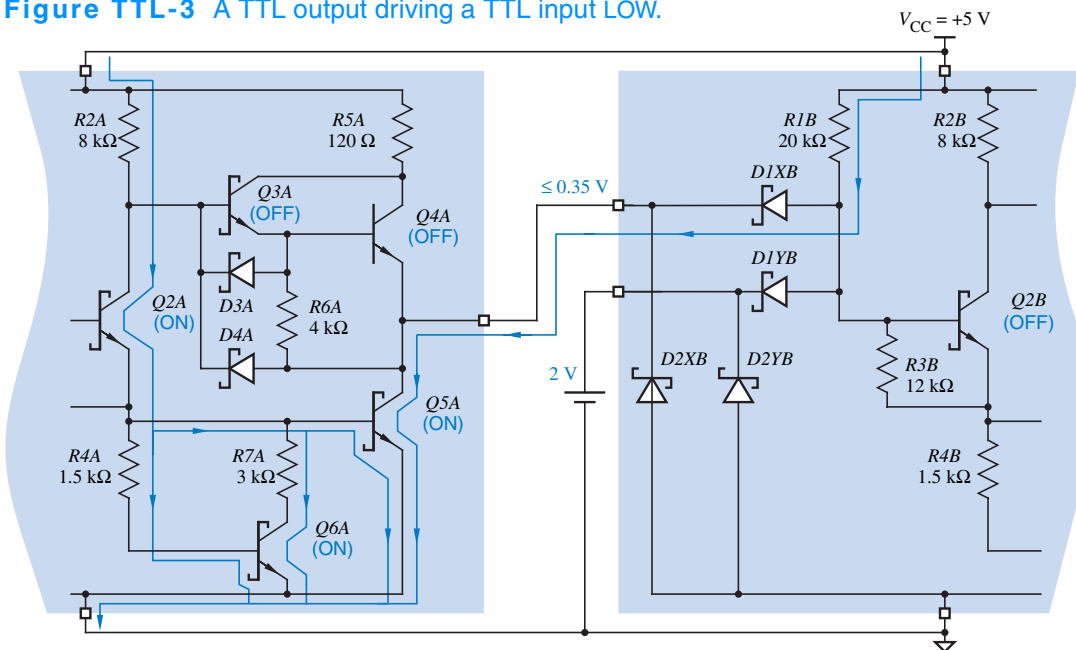
Current spikes can show up as noise on the power-supply and ground connections in TTL circuits, especially when multiple outputs are switched simultaneously. For this reason, reliable circuits require decoupling capacitors between  $V_{CC}$  and ground, distributed throughout the circuit so there is a capacitor nearby each chip. Decoupling capacitors supply the instantaneous current needed during transitions.

Since the output transistors  $Q4$  and  $Q5$  are normally complementary—one ON and the other OFF—you might question the purpose of the  $120\text{-}\Omega$  resistor  $R5$  in the output stage. A value of  $0\ \Omega$  would give even better driving capability in the HIGH state. This is certainly true from a DC point of view. However, when the TTL output is changing from HIGH to LOW or vice versa, there is a short time when both transistors may be on. The purpose of  $R5$  is to limit the amount of current that flows from  $V_{CC}$  to ground during this time. Even with a  $120\ \Omega$  resistor in the TTL output stage, higher-than-normal currents called current spikes flow when TTL outputs are switched. These are similar to the current spikes that occur when high-speed CMOS outputs switch.

So far we have shown the input signals to a TTL gate as ideal voltage sources. Figure TTL-3 shows the situation when a TTL input is driven LOW by the output of another TTL gate. Transistor  $Q5A$  in the driving gate is ON, and thereby provides a path to ground for the current flowing out of the diode  $D1XB$  in the driven gate. When current flows *into* a TTL output in the LOW state, as in this case, the output is said to be *sinking current*.

*sinking current*

**Figure TTL-3** A TTL output driving a TTL input LOW.



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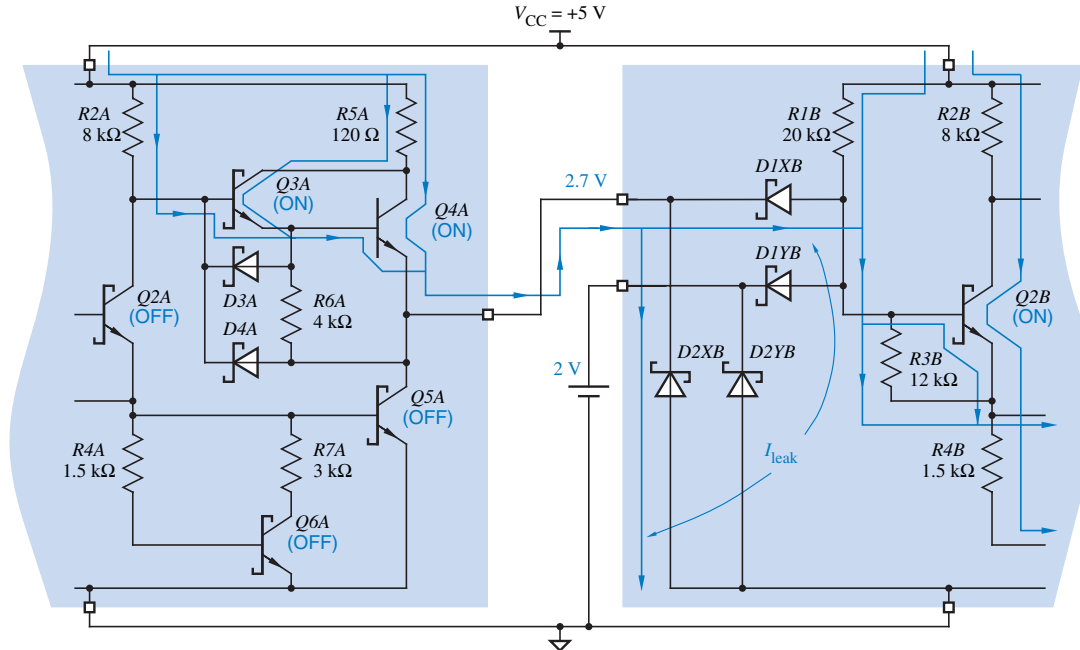


Figure TTL-4 A TTL output driving a TTL input HIGH.

Figure TTL-4 shows the same circuit with a HIGH output. In this case,  $Q4A$  in the driving gate is turned on enough to supply the small amount of leakage current flowing through reverse-biased diodes  $D1XB$  and  $D2XB$  in the driven gate. When current flows out of a TTL output in the HIGH state, the output is said to be *sourcing current*.

*sourcing current*

## TTL.2 Logic Levels and Noise Margins

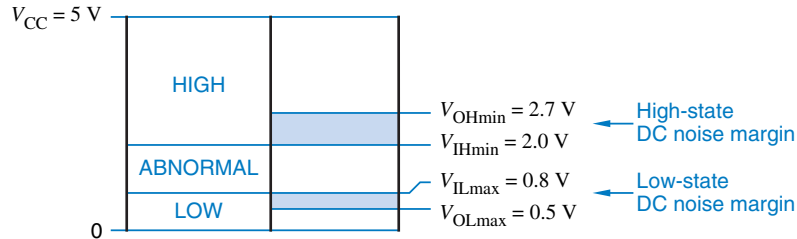
At the beginning of this section, we indicated that we would consider TTL signals between 0 and 0.8 V to be LOW, and signals between 2.0 and 5.0 V to be HIGH. Actually, we can be more precise by defining TTL input and output levels in the same way as we did for CMOS:

- $V_{OHmin}$  The minimum output voltage in the HIGH state, 2.7 V for most TTL families.
- $V_{IHmin}$  The minimum input voltage guaranteed to be recognized as a HIGH, 2.0 V for all TTL families.
- $V_{ILmax}$  The maximum input voltage guaranteed to be recognized as a LOW, 0.8 V for most TTL families.
- $V_{OLmax}$  The maximum output voltage in the LOW state, 0.5 V for most families.

These noise margins are illustrated in Figure TTL-5.

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**Figure TTL-5**  
Noise margins for popular TTL logic families (74LS, 74S, 74ALS, 74AS, 74F).

In the HIGH state, the  $V_{OHmin}$  specification of most TTL families exceeds  $V_{IHmin}$  by 0.7 V, so TTL has a *DC noise margin* of 0.7 V in the HIGH state. That is, it takes at least 0.7 V of noise to corrupt a worst-case HIGH output into a voltage that is not guaranteed to be recognizable as a HIGH input. In the LOW state, however,  $V_{ILmax}$  exceeds  $V_{OLmax}$  by only 0.3 V, so the DC noise margin in the LOW state is only 0.3 V. In general, TTL and TTL-compatible circuits tend to be more sensitive to noise in the LOW state than in the HIGH state.

*DC noise margin*

### TTL.3 Fanout

As we defined it previously in Section 3.5.4, *fanout* is a measure of the number of gate inputs that are connected to (and driven by) a single gate output. As we showed in that section, the DC fanout of CMOS outputs driving CMOS inputs is virtually unlimited, because CMOS inputs require almost no current in either state, HIGH or LOW. This is not the case with TTL inputs. As a result, there are very definite limits on the fanout of TTL or CMOS outputs driving TTL inputs, as you'll learn in the paragraphs that follow.

*fanout*

As in CMOS, the *current flow* in a TTL input or output lead is defined to be positive if the current actually flows *into* the lead, and negative if current flows *out* of the lead. As a result, when an output is connected to one or more inputs, the algebraic sum of all the input and output currents is 0.

*current flow*

The amount of current required by a TTL input depends on whether the input is HIGH or LOW, and is specified by two parameters:

$I_{ILmax}$  The maximum current that an input requires to pull it LOW. Recall from the discussion of Figure TTL-3 that positive current is actually flowing from  $V_{CC}$ , through  $R1B$ , through diode  $D1XB$ , out of the input lead, through the driving output transistor  $Q5A$ , and into ground.

Since current flows out of a TTL input in the LOW state,  $I_{ILmax}$  has a negative value. Most LS-TTL inputs have  $I_{ILmax} = -0.4$  mA, which is sometimes called a *LOW-state unit load* for LS-TTL.

*LOW-state unit load*

$I_{IHmax}$  The maximum current that an input requires to pull it HIGH. As shown in Figure TTL-4, positive current flows from  $V_{CC}$ , through  $R5A$  and  $Q4A$  of the driving gate, and *into* the driven input, where it leaks to ground through reverse-biased diodes  $D1XB$  and  $D2XB$ .

Since current flows *into* a TTL input in the HIGH state,  $I_{IHmax}$  has a positive value. Most LS-TTL inputs have  $I_{IHmax} = 20 \mu\text{A}$ , which is sometimes called a *HIGH-state unit load* for LS-TTL.

*HIGH-state unit load*

Like CMOS outputs, TTL outputs can source or sink a certain amount of current depending on the state, HIGH or LOW:

$I_{OLmax}$  The maximum current an output can sink in the LOW state while maintaining an output voltage no more than  $V_{OLmax}$ . Since current flows into the output,  $I_{OLmax}$  has a positive value, 8 mA for most LS-TTL outputs.

$I_{OHmax}$  The maximum current an output can source in the HIGH state while maintaining an output voltage no less than  $V_{OHmin}$ . Since current flows out of the output,  $I_{OHmax}$  has a negative value,  $-400 \mu\text{A}$  for most LS-TTL outputs.

Notice that the value of  $I_{OLmax}$  for typical LS-TTL outputs is exactly 20 times the absolute value of  $I_{ILmax}$ . As a result, LS-TTL is said to have a *LOW-state fanout* of 20, because an output can drive up to 20 inputs in the LOW state. Similarly, the absolute value of  $I_{OHmax}$  is exactly 20 times  $I_{IHmax}$ , so LS-TTL is said to have a *HIGH-state fanout* of 20 also. The *overall fanout* is the lesser of the LOW- and HIGH-state fanouts.

*LOW-state fanout*

*HIGH-state fanout*  
*overall fanout*

Loading a TTL output with more than its rated fanout has the same deleterious effects that were described for CMOS devices in Section 3.5.5 on page 111. That is, DC noise margins may be reduced or eliminated, transition times and delays may increase, and the device may overheat.

In general, two calculations must be carried out to confirm that an output is not being overloaded:

**HIGH state** The  $I_{IHmax}$  values for all of the driven inputs are added. This sum must be less than or equal to the absolute value of  $I_{OHmax}$  for the driving output.

#### **TTL OUTPUT ASYMMETRY**

Although LS-TTL's numerical fanouts for HIGH and LOW states are equal, LS-TTL and other TTL families have asymmetric current driving capability—an LS-TTL output can sink 8 mA in the LOW state, but can source only  $400 \mu\text{A}$  in the HIGH state.

This asymmetry is no problem when TTL outputs drive other TTL inputs, because it is matched by a corresponding asymmetry in TTL input current requirements ( $I_{ILmax}$  is large, while  $I_{IHmax}$  is small). However, it is a limitation when TTL is used to drive LEDs, relays, solenoids, or other devices requiring large amounts of current, often tens of milliamperes. Circuits using these devices must be designed so that current flows (and the driven device is “on”) when the TTL output is in the LOW state, and so little or no current flows in the HIGH state. Special TTL buffer/driver gates are made that can sink up to 60 mA in the LOW state, but that still have a rather puny current-sourcing capability in the HIGH state (2.4 mA).

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**BURNED FINGERS** If a TTL or CMOS output is forced to sink a lot more than  $I_{OLmax}$ , the device may be damaged, especially if high current is allowed to flow for more than a second or so. For example, suppose that a TTL output in the LOW state is short-circuited directly to the 5 V supply. The ON resistance,  $R_{CE(sat)}$ , of the saturated  $Q5$  transistor in a typical TTL output stage is less than  $10\ \Omega$ . Thus,  $Q5$  must dissipate about  $5^2/10$  or 2.5 watts. Don't try this yourself unless you're prepared to deal with the consequences! That's enough heat to destroy the device (and burn your finger) in a very short time.

**LOW state** The  $I_{ILmax}$  values for all of the driven inputs are added. The absolute value of this sum must be less than or equal to  $I_{OLmax}$  for the driving output.

For example, suppose you designed a system in which a certain LS-TTL output drives ten LS-TTL and three S-TTL gate inputs. In the HIGH state, a total of  $10 \cdot 20 + 3 \cdot 50\ \mu A = 350\ \mu A$  is required. This is within an LS-TTL output's HIGH-state current-sourcing capability of  $400\ \mu A$ . But in the LOW state, a total of  $10 \cdot 0.4 + 3 \cdot 2.0\ mA = 10.0\ mA$  is required. This is more than an LS-TTL output's LOW-state current-sinking capability of  $8\ mA$ , so the output is overloaded.

#### TTL.4 Unused Inputs

Unused inputs of TTL gates can be handled in the same way as we described for CMOS gates in Section 3.5.6 on page 112. That is, unused inputs may be tied to used ones, or unused inputs may be pulled HIGH or LOW as is appropriate for the logic function.

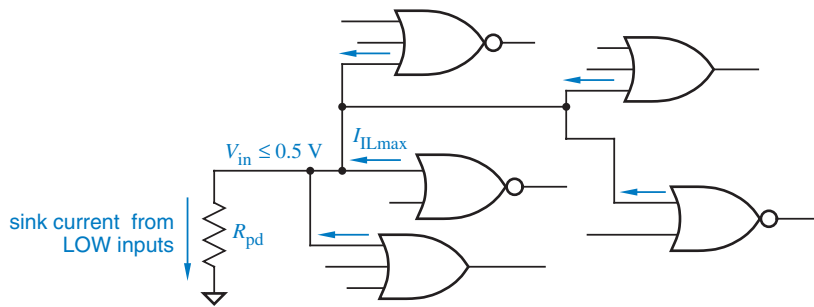
The resistance value of a pull-up or pull-down resistor is more critical with TTL gates than CMOS gates, because TTL inputs draw significantly more current, especially in the LOW state. If the resistance is too large, the voltage drop across the resistor may result in a gate input voltage beyond the normal LOW or HIGH range.

For example, consider the pull-down resistor shown in Figure TTL-6. The pull-down resistor must sink  $0.4\ mA$  of current from each of the unused LS-TTL inputs that it drives. Yet the voltage drop across the resistor must be no more than

**FLOATING TTL INPUTS** Analysis of the TTL input structure shows that unused inputs left unconnected (or *floating*) behave as if they have a HIGH voltage applied—they are pulled HIGH by base resistor  $R1$  in Figure TTL-1. However,  $R1$ 's pull-up is much weaker than that of a TTL output driving the input. As a result, a small amount of circuit noise, such as that produced by other gates when they switch, can make a floating input spuriously behave like it's LOW. Therefore, for the sake of reliability, unused TTL inputs should be tied to a stable HIGH or LOW voltage source.

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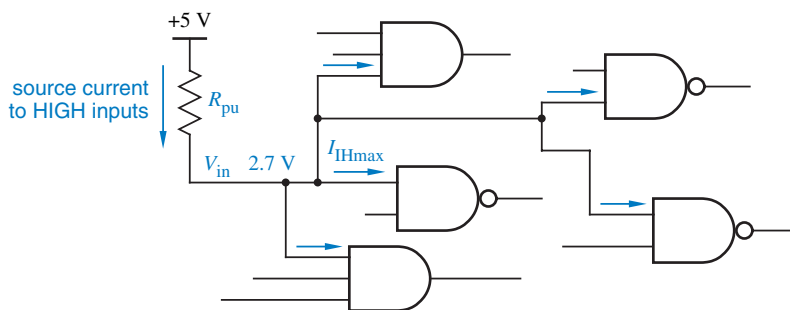
**Figure TTL-6**  
Pull-down resistor for TTL inputs.

0.5 V in order to have a LOW input voltage no worse than that produced by a normal gate output. If the resistor drives  $n$  LS-TTL inputs, then we must have

$$n \cdot 0.4 \text{ mA} \cdot R_{pd} < 0.5 \text{ V}$$

Thus, if the resistor must pull 10 LS-TTL inputs LOW, then we must have  $R_{pd} < 0.5 / (10 \cdot 0.4 \cdot 10^{-3})$ , or  $R_{pd} < 125 \Omega$ .

Similarly, consider the pull-up resistor shown in Figure TTL-7. It must source  $20 \mu\text{A}$  of current to each unused input while producing a HIGH voltage no worse than that produced by a normal gate output, 2.7 V. Therefore, the voltage



**Figure TTL-7**  
Pull-up resistor for TTL inputs.

**WHY USE A RESISTOR?**

You might be asking yourself, “Why use a pull-up or pull-down resistor, when a direct connection to ground or the 5-V power supply should be a perfectly good source of LOW or HIGH?”

Well, for a HIGH source, a direct connection to the 5-V power supply is not recommended, since an input transient of over 5.5 V can damage some TTL devices, ones that use a multiple-emitter transistor in the input stage. The pull-up resistor limits current and prevents damage in this case.

For a LOW source, a direct connection to ground without the pull-down resistor is actually OK in most cases. You’ll see many examples of this sort of connection throughout this book. However, as we show in [Section DFT.2](#), the pull-down resistor is still desirable in some cases, so that the “constant” LOW signal it produces can be overridden and driven HIGH for system-testing purposes.



drop across the resistor must be no more than 2.3 V; if  $n$  LS-TTL input are driven, we must have

$$n \cdot 20 \mu A \cdot R_{pu} < 2.3 \text{ V}$$

Thus, if 10 LS-TTL inputs are pulled up, then  $R_{pu} < 2.3 / (10 \cdot 20 \cdot 10^{-6})$ , or  $R_{pu} < 11.5 \text{ k}\Omega$

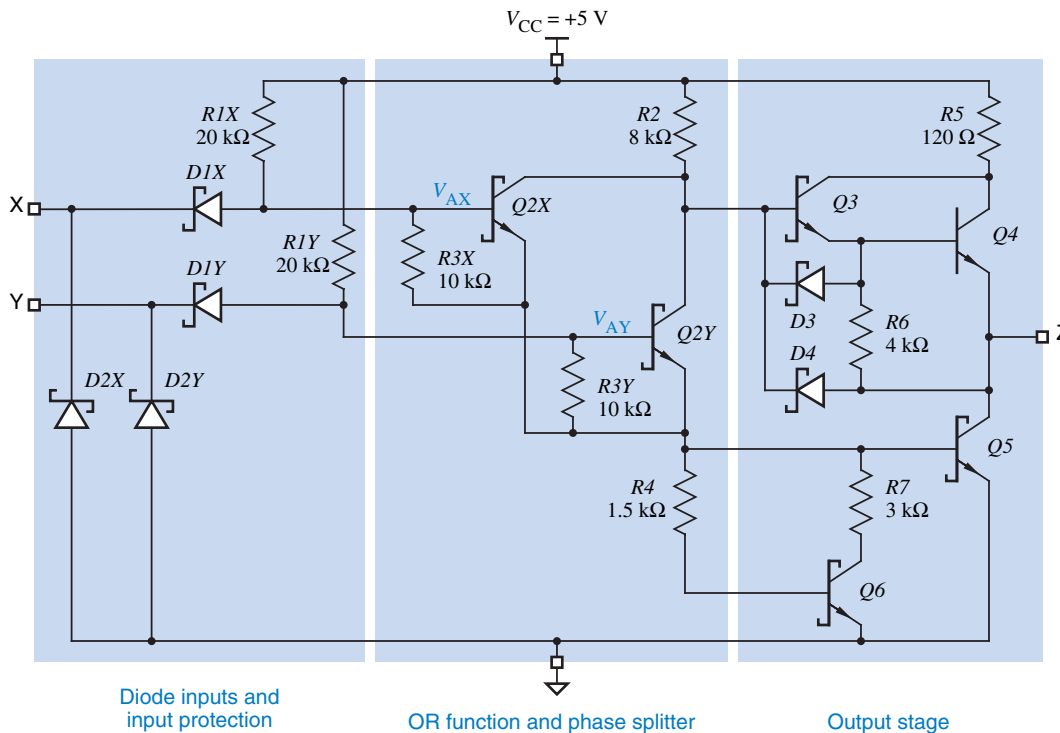
### TTL.5 Additional TTL Gate Types

Although the NAND gate is the “workhorse” of the TTL family, other types of gates can be built with the same general circuit structure.

The circuit diagram for an LS-TTL NOR gate is shown in Figure TTL-8. If either input X or Y is HIGH, the corresponding phase-splitter transistor  $Q2X$  or  $Q2Y$  is turned on, which turns off  $Q3$  and  $Q4$  while turning on  $Q5$  and  $Q6$ , and the output is LOW. If both inputs are LOW, then both phase-splitter transistors are off, and the output is forced HIGH. This functional operation is summarized in Figure TTL-9 on the next page.

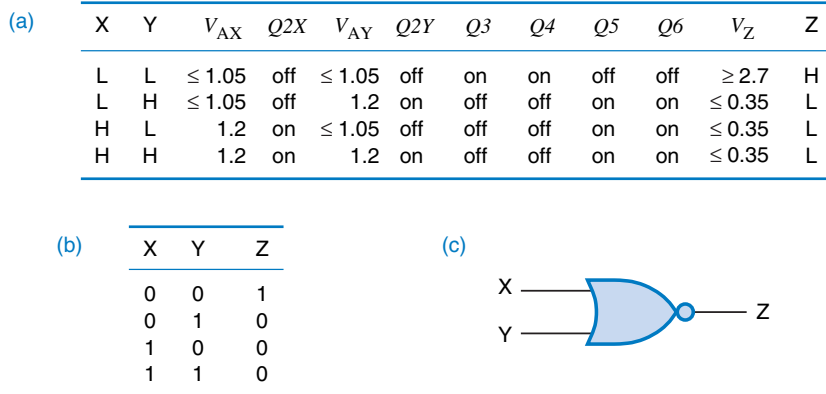
The LS-TTL NOR gate’s input circuits, phase splitter, and output stage are almost identical to an LS-TTL NAND gate’s. The difference is that an LS-TTL NAND gate uses diodes to perform the AND function, while an LS-TTL NOR gate uses parallel transistors in the phase splitter to perform the OR function.

**Figure TTL-8** Circuit diagram of a 2-input LS-TTL NOR gate.



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**Figure TTL-9**  
A 2-input LS-TTL NOR gate:  
(a) function table;  
(b) truth table;  
(c) logic symbol.

The speed, input, and output characteristics of a TTL NOR gate are comparable to those of a TTL NAND. However, an  $n$ -input NOR gate uses more transistors and resistors and is thus more expensive in silicon area than an  $n$ -input NAND. Also, internal leakage current limits the number of  $Q2$  transistors that can be placed in parallel, so NOR gates have poor fan-in. (The largest discrete TTL NOR gate has only 5 inputs, compared with a 13-input NAND.) As a result, NOR gates are less commonly used than NAND gates in TTL designs.

The most “natural” TTL gates are inverting gates like NAND and NOR. Noninverting TTL gates include an extra inverting stage, typically between the input stage and the phase splitter. As a result, noninverting TTL gates are typically larger and slower than the inverting gates on which they are based.

Like CMOS, TTL gates can be designed with three-state outputs. Such gates have an “output-enable” or “output-disable” input that allows the output to be placed in a high-impedance state where neither output transistor is turned on.

Some TTL gates are also available with *open-collector outputs*. Such gates omit the entire upper half of the output stage in Figure TTL-1, so that only passive pull-up to the HIGH state is provided by an external resistor. The applications and required calculations for TTL open-collector gates are similar to those for CMOS gates with open-drain outputs.

*open-collector output*

## Exercises

- TTL.1** Discuss the key benefit and the key drawback of Schottky transistors in TTL.
- TTL.2** Discuss the pros and cons of larger vs. smaller pull-up resistors for open-collector TTL outputs.
- TTL.3** When comparing the TTL NOR gate to the TTL NAND gate, which of the following characteristics are true of the NOR gate: slower, uses more silicon, poor fan-in, uses diode logic.
- TTL.4** Assuming “ideal” conditions, what is the minimum voltage that will be recognized as a HIGH in the TTL NAND gate in Figure TTL-1 with one input LOW and the other HIGH?

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- TTL.5** Assuming “ideal” conditions, what is the maximum voltage that will be recognized as a LOW in the TTL NAND gate in Figure TTL-1 with both inputs HIGH?
- TTL.6** Find a commercial TTL part that can source 40 mA in the HIGH state. What is its application?
- TTL.7** What happens if you try to drive an LED with its cathode grounded and its anode connected to a TTL totem-pole output, analogous to Figure 3-54(b) for CMOS?
- TTL.8** What happens if you try to drive a 12-volt relay with a TTL totem-pole output?
- TTL.9** Suppose that a single  $7.5\text{K } \Omega$  pull-up resistor to +5 V is used to provide a constant-1 logic source to 20 different 74LS00 inputs. How much HIGH-state DC noise margin are you providing in this case? What is the maximum value of this resistor if we want a HIGH-state DC noise margin of 1V?
- TTL.10** The circuit in Figure xTTL.10 uses open-collector NAND gates to perform “wired logic.” Write a truth table for output signal F and, if you’ve read Section 4.2, a logic expression for F as a function of the circuit inputs.
- TTL.11** What is the maximum allowable value for  $R1$  in Figure xTTL.10? Assume that a 0.6-V HIGH-state noise margin is required. The 74LS01 has the specs shown in the 74LS column of Table 3-10, except that  $I_{OHmax}$  is  $100 \mu\text{A}$ , a leakage current that flows *into* the output in the HIGH state.
- TTL.12** Suppose that the output signal F in Figure xTTL.10 drives the inputs of three 74S04 inverters. Compute the minimum and maximum allowable values of  $R2$ , assuming that a 0.8-V HIGH-state noise margin is required.
- TTL.13** A 74LS125 is a buffer with a three-state output. When enabled, the output can sink 24 mA in the LOW state and source 2.6 mA in the HIGH state. When disabled, the output has a leakage current of  $\pm 20 \mu\text{A}$  (the sign depends on the output voltage—plus if the output is pulled HIGH by other devices, minus if it’s LOW). Suppose a system is designed with multiple modules connected to a bus, where each module has a single 74LS125 to drive the bus and one 74LS04 to receive information on the bus. What is the maximum number of modules that can be connected to the bus without exceeding the 74LS125’s specs?

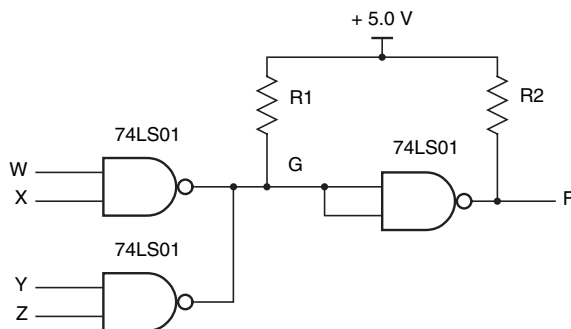


Figure xTTL.10

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- TTL.14 Repeat the preceding exercise, this time assuming that a single pull-up resistor is connected from the bus to +5 V to guarantee that the bus is HIGH when no device is driving it. Calculate the maximum possible value of the pull-up resistor, and the number of modules that can be connected to the bus.
- TTL.15 Find the circuit design in a TTL data book for an actual three-state gate, and explain how it works.
- TTL.16 Using the graphs in a TTL data book, develop some rules of thumb for derating the maximum-propagation-delay specification of LS-TTL under nonoptimal conditions of power-supply voltage, temperature, and loading.

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